Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (currently amended): A method for manufacturing a transistor, comprising:

providing a transistor assembly including a silicon based semiconductor layer with a first surface, a dielectric layer disposed on at least part of the first surface, and a gate electrode disposed on the dielectric layer, the assembly further including an insulation layer adjacent at least part of the gate electrode and a nitride spacer ~~layer~~ adjacent at least part of the insulation layer;

depositing, on a portion of the first surface, a material that will react with the semiconductor layer to form a silicide portion adjacent said nitride spacer;

removing the ~~unreacted~~ material that does not react with the portion of the first surface;

etching the nitride spacer ~~layer~~ subsequent to the removing of the material that does not react with a portion of the first surface;

depositing a pre-metal spacer layer adjacent at least part of the nitride spacer ~~layer~~ and over at least part of the ~~silicided~~ silicide portion of the first surface;

etching and removing a portion of the pre-metal spacer layer above the ~~silicided~~ silicide portion ~~of the first surface~~ to expose at least part of the ~~silicided~~ silicide portion ~~of the first surface~~; and

forming a contact with the exposed part of the ~~silicided~~ silicide portion ~~of the first surface~~ where the pre-metal spacer layer was removed.

Claim 2 (currently amended): The method of Claim 1, wherein etching the nitride spacer ~~layer~~ comprises reducing ~~the~~ a width of the nitride spacer ~~layer~~ approximately thirty nanometers.

Claim 3 (currently amended): The method of Claim 1, wherein etching the nitride spacer ~~layer~~ comprises placing the transistor assembly in an etchant.

Claim 4 (original): The method of Claim 3, wherein the etchant comprises phosphoric acid.

Claim 5 (original): The method of Claim 4, wherein the temperature of the etchant comprises approximately one-hundred and sixty degrees Celsius.

Claim 6 (currently amended): The method of Claim 4, wherein etching the nitride spacer ~~layer~~ comprises placing the transistor assembly in the etchant between approximately two to eight minutes.

Claim 7 (currently amended): The method of Claim 1, further comprising:

rinsing the transistor assembly to remove the etchant used to etch the nitride spacer ~~layer~~; and

drying the transistor assembly.

Claim 8 (original): The method of Claim 1, wherein an edge of the contact is formed between approximately forty to one-hundred and fifty nanometers from an edge of the gate electrode.

Claim 9 (original): The method of Claim 1, further comprising applying a dopant to a portion of the first surface to form a source region.

Claim 10 (original): The method of Claim 9, wherein applying a dopant comprises diffusing arsenic into the portion of the first surface.

Claim 11 (currently amended): The method of Claim 1, wherein the material used to form the silicide comprises Co ~~$CoSi_2$~~.

Claim 12 (original): The method of Claim 1, further comprising:

removing a portion of the nitride spacer layer to expose part of a surface of the insulation layer; and

removing the portion of the insulation layer below the exposed surface of the insulation layer to expose part of the first surface of the semiconductor layer.

Claim 13 (original): The method of Claim 1, further comprising:

depositing a second pre-metal spacer layer adjacent the first pre-metal spacer layer; and

etching a portion of the second pre-metal spacer layer above at least part of the silicided portion of the first surface to expose a part of a surface of the first pre-metal spacer layer.

Claim 14 (original): The method of Claim 1, wherein depositing a material that will react with the semiconductor layer to form silicide comprises depositing the material on an exposed surface of the gate electrode to form a silicided portion of the gate electrode.

Claim 15 (withdrawn): A transistor comprising:

a silicon based semiconductor layer having a first surface, at least a portion of the semiconductor layer adjacent the first surface having been silicided;

a dielectric layer disposed on at least part of the first surface;

a gate electrode disposed on the dielectric layer;

an insulation layer adjacent at least part of the gate electrode; and

a nitride spacer layer adjacent at least part of the insulation layer;

wherein the distance from an edge of the gate electrode to the beginning of the silicided portion of the semiconductor layer is greater than the distance from the edge of the gate electrode to the edge of the nitride spacer layer closest the silicided portion.

Claim 16 (withdrawn): The transistor of Claim 15, wherein the distance between the edge of the nitride spacer layer closest the silicided portion of the semiconductor layer and the beginning of the silicided portion comprises approximately thirty nanometers.

Claim 17 (withdrawn): The transistor of Claim 15, wherein the distance between the edge of the nitride spacer layer closest the silicided portion of the semiconductor layer and the beginning of the silicided portion is formed by etching the nitride spacer layer after forming the silicided portion.

Claim 18 (withdrawn): The transistor of Claim 17, wherein the etchant comprises phosphoric acid at a temperature of approximately one-hundred and sixty degrees Celsius.

Claim 19 (withdrawn): The transistor of Claim 15, wherein the material used to form the silicide comprises $CoSi_2$.

Claim 20 (withdrawn): The transistor of Claim 15, wherein the dielectric layer comprises nitrided oxide.

Claim 21 (withdrawn): The transistor of Claim 15, wherein the gate electrode comprises polycrystalline silicon.

Claim 22 (withdrawn): The transistor of Claim 15, wherein the silicided portion of the semiconductor layer has also been doped.

Claim 23 (withdrawn): The transistor of Claim 15, wherein the distance from the edge of the gate electrode to the beginning of the silicided portion of the semiconductor layer is between approximately fifty and one-hundred and sixty nanometers.

Claim 24 (withdrawn): The transistor of Claim 15, wherein a portion of the gate electrode has been silicided.

Claim 25 (withdrawn): A transistor comprising:

a silicon based semiconductor layer having a first surface, at least a portion of the semiconductor layer adjacent the first surface having been doped and silicided;

a dielectric layer comprising nitrided oxide disposed on at least part of the first surface;

a gate electrode comprising polycrystalline silicon disposed on the dielectric layer, a portion of the gate electrode having been silicided;

an insulation layer comprising oxide adjacent at least part of the gate electrode; and

a spacer layer comprising nitride adjacent at least part of the insulation layer;

wherein the distance between the edge of the spacer layer closest the silicided portion of the semiconductor layer and the beginning of the silicided portion of the semiconductor layer is more than twenty nanometers.

Amendments to the Drawings:

None